Single Mask Lithographic Process for Patterning Multiple Types of Surface Features

ABSTRACT OF THE DISCLOSURE

A method for patterning different types of surface features on a semiconductor substrate (e.g. metal pads, etched pits and grooves) where the features are accurately located by a single mask. First, a dielectric layer is formed on the substrate. Next, an etch-resistant metal layer is formed on the dielectric and patterned according to a mask. Then, a patterned resist mask (e.g. PMMA) is formed on the patterned metal so that areas of the dielectric are exposed. The resist mask has edges that lie on top of the patterned metal layer. Therefore, the exposed dielectric areas are bounded by patterned metal. Then, the dielectric layer is etched using a directional dry etch to expose the underlying semiconductor substrate. Then, the semiconductor substrate is etched. The dielectric layer functions as a mask in the substrate etching step. Since the metal pattern determines the areas of the substrate that are etched, all the features are located according to the original mask that defined the metal pattern. Subsequent masking steps can expose other areas of the substrate to different etching or deposition processes.